floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first side wall;

an erase gate formed over a second one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said second one of said side walls by said second insulation layer;

a drain region formed in a portion of said substrate proximate said control gate; and

a source region formed in a portion of said substrate proximate said erase gate;

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

2. (Amended) A semiconductor device having at least one transistor as recited in claim 1 wherein said erase gate overlaps said floating gate and at least a portion of said control gate.

8. (Amended) A memory array disposed on a substrate comprising a plurality of memory cells each having a channel region formed in said substrate, a floating gate separated from said channel region by a first insulating layer, an erase gate, a control gate separated from said floating gate by a second insulating layer, a source region, and a drain region, comprising:

a plurality of rows and columns of interconnected memory cells wherein the control gates of memory cells in the same row are connected by a common word-line, the erase gates of the memory cells in the same rows are connected by a common erase line, the source regions of the memory cells in the same rows are connected by a common source line, and the drain regions of memory cells in the same columns are commonly connected via a common drain line, wherein at least a portion of each said control gate is disposed over a portion of said channel region and is separated therefrom by said second insulating layer, and wherein a portion of said control gate is

disposed in facing relationship to a side surface of said floating gate and is separated therefrom by said second insulating layer; and

a control circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array;

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

9. (Amended) A memory array disposed on a substrate as recited in claim 8 wherein said floating gate is generally disposed over said channel region and is separated therefrom by said first insulating layer, said control gate is generally placed on one side of said floating gate and separated therefrom by said second insulation layer, said erase gate is generally placed on a second side of said floating gate and is separated therefrom by said second insulation layer, said drain region is generally disposed on said one side of said floating gate, and said source region is generally disposed on said second side of said floating gate.

10. (Amended) A memory array as recited in claim 9 wherein said erase gate overlaps said floating gate and at least a portion of said control gate.

16. (Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region;

a first insulating layer disposed over said channel region and over at least a portion ~~of~~ said substrate;

a floating gate generally disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a portion of said channel region and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first one of said side walls;

an erase gate formed over a second one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said second one of said side walls by said second insulation layer;

a source region formed in a portion of said substrate proximate said erase gate; and a drain region formed in a portion of said substrate proximate said control gate;

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

17. (Amended) A semiconductor device having at least one transistor as recited in claim 16 wherein said erase gate is disposed over at least a portion of each of said floating gate and said control gate.

Add the following new claims:

18. (New) A semiconductor memory cell formed on a substrate, comprising:

a source region formed in said substrate;

first and second drain regions respectively formed in said substrate in spaced apart relationship to and on opposite sides of said source region;

a first channel region disposed between said first drain region and said source region, and a second channel region disposed between said source region and said second drain region;

a first floating gate having at least a substantial portion thereof disposed over said first channel region and separated therefrom by a first insulation layer, and a second floating gate having at least a substantial portion thereof disposed over said second channel region and separated therefrom by said first insulation layer;

an erase gate overlying said source region and having opposite extremities thereof extending over at least portions of said first and second floating gates; and

a first control gate having a first portion overlying said first channel region and a second portion overlying a portion of said first floating gate; and

a second control gate having a first portion overlying said second channel region and a second portion overlying a portion of said second floating gate;

whereby with said drain regions and erase gates grounded, a relatively high potential applied to said source region, and a relatively low potential applied to said control gates, the floating gates will be coupled to the high potential at the source region, and hot carriers produced in the channel regions under the floating gates and first portions of the control gates will be injected into the floating gates; and

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

19.(New) A memory cell as recited in claim 18 wherein each said floating gate has at least two side walls, and each said control gate has a third portion facing one of said side walls.

20. (New) A memory cell as recited in claim 19 wherein said erase gate has portions facing the other one of the sidewalls of each said floating gate.

Sub F2

D4 end

21. (New) A memory cell as recited in claim 18 wherein each said floating gate has at least two side walls, and said erase gate has portions facing one of the side walls of each said floating gate.

22. (New) A memory cell as recited in claim 18 wherein said opposite extremities of said erase gate extend across said floating gates to overly portions of said first and second control gates.